UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,966	10/24/2003	Khader S. Abdel-Hafez	3359-Z	6973

7590 09/13/2005

Law Office of Jim Zegeer
Suite 108
801 North Pitt Street
Alexandria, VA 22314

EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,966	ABDEL-HAFEZ ET AL.	
	Examiner	Art Unit	
	John P. Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *83-106* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *83-106* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the applicant's amendment and RCE dated 7/19/2005.

The applicant canceled claims 1-82.

Claims 83-106 were added as new.

Claims 83-106 are pending.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/19/2005 has been entered.

Priority

2. Domestic Priority Not Granted:

Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged. However, the provisional application upon which priority is claimed fails to provide adequate support under 35 U.S.C. 112 for claims 83-106 of this application. The lack of support in the provisional application is in reference to global scan enable and global set/reset enable signals being used to control the set/reset controller.

Information Disclosure Statement

3. The examiner has considered the applicant's Information Disclosure Statement dated 8/20/2004.

Response to Amendment

4. In view of the applicant's amendments to the Specification, and the changes to the Drawings, the examiner withdraws all objections to the said Specification and Drawings communicated in the examiner's previous office action of 4/5/2005.

5. In view of the applicant's cancellation of Claims 1-82, the examiner withdraws all rejections of said claims because the claims are moot. The office action continues below with further prosecution of the new claims.

Claim Rejections - 35 USC § 103

6. Claims 83-106 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahanin et al., U.S. Patent No. 5166604 (herein Ahanin), in view of the applicant's admitted prior art (herein AAPA), in view of Wang et al., U.S. Patent Application No. 2002/0120896 (herein Wang), and further in view of "ORCA® Series 4 FPGAs" by Lattice Semiconductor (herein Lattice).

As per Claims 83, 91 and 96:

Ahanin teaches a method for testing faults propagated to the data ports asynchronous set/reset ports of scan cells in an integrated circuit based on a set/reset

controller (FIG.2,4) having a scan enable signal and a set/reset enable signal for testing faults propagated to the data ports and asynchronous set/reset ports of selected scan cells (see Background of Ahanin) in a scan-based integrated circuit (see FIG.2), the scan-based integrated circuit containing one or more set/reset circuitries (FIG.2 102, 112) and one or more scan chains (for example column 2 lines 22-52 and FIG.1), each scan chain comprising multiple scan cells coupled in series (see example of FIG.1), each scan cell having one or more clocks (FIG.2 12f, 12i); but Ahanin fails to further teach said set/reset controller comprising shift and capture controllers. But in the AAPA, the features are disclosed as follows;

a shift controller (AAPA FIG.2D 262), inserted between a selected set/reset circuitry (FIG.2D 203) and said asynchronous set/reset ports of all said selected scan cells (FIG.2D 205), for disabling said asynchronous set/reset ports of all said selected scan cells (FIG.2D 262), when said scan enable signal is enabled (in FIG.2D, the AND performs the function), during a shift-in or shift-out operation (SE used for shifting is obvious because it is well known in the art); and

a capture controller (AAPA FIG.2E 281), inserted between said selected set/reset circuitry (FIG.2E 203) and said asynchronous set/reset ports of all said selected scan cells (FIG.2E 205), for enabling or disabling propagation of said faults present in said selected set/reset circuitry to said asynchronous set/reset ports of all said selected scan cells, in response to said set/reset enable signal when said scan enable signal is disabled (in FIG.2E, the multiplexer 281 performs the function), during a capture operation (SE disablement is an obvious and well known occurrence during capture).

Motivation for the combination of the AAPA with Ahanin comes from the advantages stated in the applicant's Background statement on page 6, as advantageously detecting set/reset faults during scan testing and capture cycles. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include shift and capture circuits as described in the AAPA to the controls of Ahanin in order to improve set/reset detection capabilities in a scan circuit.

However, neither Ahanin nor the AAPA provide a disclosure wherein the set/reset enable and the scan enable signals are in fact global signals. However, a teaching that each signal is in fact disclosed as being global is incorporated into the analogous art references of Lattice (Global Set/Reset Enable) on pages 36 in Table 16, and page 61 column 1 last paragraph, and Wang (for example FIG.2 201, Global Scan Enable). Lattice boasts of new features and enhancements not available earlier in the Introduction, and Wang, in paragraph [0011] states the disadvantage of complex scan enable requirements is supplanted by a simpler approach resulting in the advantageous use of a global scan enable (paragraph [0017]. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to incorporate the improvements of Lattice and Wang with Ahanin and the AAPA in order to enhance set/reset testing along with improved and simpler circuitry (a global signal) for scan enable.

As per Claim 84:

Wang further teaches the method of claim 83, wherein said shifting in a stimulus to all said scan cells further comprises selectively shifting a predetermined stimulus

from an ATE (automatic test equipment) in said selected scan-test mode (Wang, paragraph [0008]) or shifting in a pseudo-random stimulus automatically generated in said scan-based integrated circuit using a pseudo-random pattern generator (PRPG) in said selected self-test mode during said shift-in operation (not elected by examiner). And in view of the motivation previously stated, the claim is rejected.

As per Claims 85 and 98:

Ahanin further teaches the set/reset controller and method of claim 83 or 96, wherein said global scan enable (global SE) signal is further used to enable shifting a scan data from a first scan cell to a second scan cell during said shift-in and said shift-out operation (for example, Ahanin, column 3 lines 29-47). And in view of the motivation previously stated, the claims are rejected.

As per Claims 86 and 99:

Ahanin further discloses the set/reset controller and method of claim 83 or 96, wherein said capture controller further comprises disabling all said clocks controlling all said scan cells, while enabling said global set/reset enable (global SR EN) signal, for testing said faults propagated to said asynchronous set/reset ports of all said selected scan cells during said capture operation (column 5 lines 1-11). And in view of the motivation previously stated, the claims are rejected.

As per Claim 87:

Ahanin further discloses the method of claim 86, wherein said enabling all said selected global set/reset enable (global SR EN) signals further comprises selectively enabling two or more said selected global set/reset enable (global SR EN) signals

simultaneously or in an ordered sequence during said capture operation (column 2 lines 46-50). And in view of the motivation previously stated, the claim is rejected.

As per Claims 88 and 100:

Ahanin further discloses the set/reset controller and method of claim 83 and 96, wherein said capture controller further comprises enabling all said clocks controlling said scan cells, while disabling said global set/reset enable (global SR EN) signal, for testing said faults propagated to said data ports of said selected scan cells during said capture operation (column 4 lines 64-68). And in view of the motivation previously stated, the claims are rejected.

As per Claims 89 and 101:

Wang further discloses the method or set/reset controller of claim 88 or 100, wherein said enabling all said clocks controlling all said scan cells further comprises selectively enabling two or more said clocks controlling two or more said scan cells simultaneously or in an ordered sequence during said capture operation (FIG.7 sheet 2 or sheet 3). And in view of the motivation previously stated, the claims are rejected.

As per Claim 90:

Wang further teaches the method of claim 83, wherein said shifting out said test response for comparison or compaction further comprises selectively shifting out said test response to said ATE for comparison in said selected scan-test mode (see Claim 80 and paragraph [0008]) or shifting out said test response for compaction using a compactor, including a multiple-input signature register (MISR), in said selected self-test

mode during said shift-out operation (not elected by examiner). And in view of the motivation previously stated, the claim is rejected.

As per Claims 92 and 103:

Wang further teaches the method or set/reset controller of claim 83 or 96, wherein said global scan enable (global SE) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit (Wang, Claim 14). And in view of the motivation previously stated, the claims are rejected.

As per Claim 93 and 104:

Lattice further teaches the method or set/reset controller of claim 83 or 96, wherein said global set/reset enable (global SR EN) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit (lattice page 32 column 1 paragraph 3). And in view of the motivation previously stated, the claims are rejected.

As per Claim 94 and 105:

Ahanin further teaches the method or set/reset controller of claim 83 or 96, wherein said scan cell is selectively a multiplexed-type D flip-flop (FIG.1), a two-port D flip-flop, or a LSSD (level-sensitive scan design) SRL (shift register latch). And in view of the motivation previously stated, the claims are rejected.

As per Claim 95 and 106:

The AAPA further discloses the method or set/reset controller of claim 83 or 96, wherein said set/reset controller is used to repair one or more asynchronous set/reset violations, comprising sequentially-gated set/reset violations (AAPA paragraph [0009] of

published application), combinationally-gated set/reset violations (non-elected), generated set/reset violations (non-elected), and destructive set/reset violations (non-elected), in a selected set/reset circuitry in said scan-based integrated circuit. And in view of the motivation previously stated, the claims are rejected.

As per Claim 97:

The AAPA further discloses the set/reset controller of claim 96, wherein said shift controller is selectively embedded in said selected set/reset circuitry or in all said selected scan cells (FIG. 2D), and wherein said global scan enable (global SE) signal (FIG. 2D 263), said global set/reset enable (global SR EN) signal (FIG. 2E 282), or said global scan enable (global SE) signal and said global set/reset enable (global SR EN) signal can be selectively used to disable all said asynchronous set/reset ports of all said selected scan cells during said shift-in or said shift-out operation (the figures 2D and 2E operate as claimed by virtue of their construction). And in view of the motivation previously stated, the claim is rejected.

As per Claim 102:

The AAPA teaches the set/reset controller of claim 96, wherein said capture controller is selectively embedded in said selected set/reset circuitry (see FIG.2D or 2E) or in all said selected scan cells. And in view of the motivation previously stated, the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100